# Transistor-Level Synthesis of Pipeline Analog-to-Digital Converters Using a Design-Space Reduction Algorithm

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***Abstract*—A novel transistor-level synthesis procedure for pipeline ADCs is presented. This procedure is able to directly map high-level converter specifications onto transistor sizes and biasing conditions. It is based on the combination of behavioral models for performance evaluation, optimization routines to minimize the power and area consumption of the circuit solution, and an algorithm to efficiently constraint the converter design space. This algorithm precludes the cost of lengthy bottom-up verifications and speeds up the synthesis task. The approach is herein demonstrated via the design of a 0.13 $\mu$m CMOS 10 bits@60 MS/s pipeline ADC with energy consumption per conversion of only 0.54 pJ@1 MHz, making it one of the most energy-efficient 10-bit video-rate pipeline ADCs reported to date. The computational cost of this design is of only 25 min of CPU time, and includes the evaluation of 13 different pipeline architectures potentially feasible for the targeted specifications. The optimum design derived from the synthesis procedure has been fine tuned to support PVT variations, laid out together with other auxiliary blocks, and fabricated. The experimental results show a power consumption of 23 mW@1.2 V and an effective resolution of 9.47-bit@1 MHz. Bearing in mind that no specific power reduction strategy has been applied; the mentioned results confirm the reliability of the proposed approach.**

***Index Terms*—Design methodology, pipeline data converters.**

## I. Introduction

THE SYNTHESIS of complex analog and mixed-signal integrated circuits (understood as the mapping of high-level specs onto independent design variables) is an extremely difficult task. Basic reasons are the large number of specs and design variables involved, the highly nonlinear nature of the relationships among these specs and variables, the fact that these relationships are interdependent, etc. [1]. Procedures for addressing the challenges of mixed-signal synthesis include *hierarchical decomposition* [2], [3], *behavioral modeling* [4]–[8], *top-down mapping* of specs, *bottom-up model refinement*, and intensive *optimization* [4], [9]–[14]. Synthesis is typically completed through a progressive, top-down, spec-mapping process which spans different mathematical representations (*levels*) of the system being synthesized to finally obtain *component* (transistors, capacitors, etc.) sizes and bias currents and voltages.

Although conceptually simple and tidy, the conventional top-down approach has practical limitations, namely, the following.

- Since top-down mapping of specs between adjacent levels of the hierarchy relies on simplified models [7], [13], [14], extensive bottom-up verifications and back-and-forth refinements are required, often leading to long iteration cycles.
- Multiple optimization processes, at least one per hierarchical level, must be run during the synthesis flow [11]. Also, as long as bottom-up verifications call for modifications of the building block specs, several optimization runs may be needed at the lower levels of the hierarchy.
- Topology generation (i.e., the selection of the circuit architecture which optimally fits given specs) uses either simplified system representations [11], [14], or heuristic techniques [13]. In any case, descriptions scarcely account for technological data what may hence lead to nonoptimal or even unfeasible solutions.
- Low-level physical variables (e.g., parasitics) are either ignored or roughly estimated in the models employed at high hierarchical levels [7], [13], [14]. To anticipate the negative impact of these parasitics, building blocks are commonly *oversized* what precludes obtaining optimum solutions in terms of area, speed, and power.

This paper overcomes these drawbacks by addressing one of the fundamental challenges of analog sizing, namely, the very large dimension of the design space. Thus, optimization is realized at behavioral level by searching in a space of just three dimensions. After optimum values of these variables are calculated, a *design space reduction* (DSR) algorithm expands the design space to obtain component sizes and biasing conditions. This expansion employs precalculated look-up tables characterizing the chosen technology.

The fact that only three variables are explored during optimization largely relaxes the computational demand of the optimization process. Also, as demonstrated by the results in the paper, the reduction of the design space dimensions is not detrimental of the accuracy of the sized solutions. Quite on the contrary, silicon prototypes yielding very low values of the figure of merit (FOM) are obtained in deep-submicrometer technologies.

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The proposed DSR algorithm is combined with an event-driven *behavioral simulator*, based on [4], [15], within a Matlab-Simulink synthesis toolbox, called SNYRCOS (Simulation-based NYquist-Rate Converter Synthesis). Although this paper focuses on pipeline analog-to-digital converters (ADCs) [13]–[18], the techniques in SNYRCOS can be reused for other Nyquist-rate converters (flash, semiflash, successive approximation register architectures, or algorithmic) and for oversampled converters.

Owing to the computational efficiency of the proposed DSR algorithm and the accuracy of the embedded behavioral simulator, SNYRCOS attains the following improvements as compared to prior art.

- High- and low-level mapping of specifications are combined into a one-leap mapping process, thereby drastically reducing the number of iterations and hence the duration of the design cycle. A single optimization run suffices to obtain the final solution.
- Transistor-level parameters, including parasitics, are accurately estimated and incorporated into high-level representations, thereby yielding a reduction of the number of bottom-up iterations needed to reach a feasible solution.
- Several alternative converter topologies can be explored down to transistor level, thereby allowing detailed architecture comparison and hence sounded architectural selection.
- Designs cycles to guarantee correct circuit performance under process, voltage, and temperature (PVT) variations only take a few minutes.

The paper is organized as follows. Section II outlines the SNYRCOS synthesis methodology and the role of the DSR algorithm. Section III shows that only three independent variables per pipeline stage are required to fully size the converter at transistor level. The section also describes the mapping constraints and algorithms used to derive the transistor sizes and biasing conditions pertaining to the building blocks of the ADC. In Section IV the proposed methodology is applied to the design of a 10 bits@60 MS/s pipeline ADC in 130 nm CMOS technology. Results in this section show very close agreement between behavioral level and transistor level simulations. Measurements from the silicon prototype are also in close agreement with simulations. Furthermore, this silicon prototype features state-of-the-art performance specs thus demonstrating adequacy of the algorithm and methods presented in the paper. Finally, Section V concludes the paper.

## II. Synthesis Tool for Pipeline ADCs

Fig. 1(a) shows the basic flow diagram of SNYRCOS consisting of four basic computational blocks, namely: a *topology generator*, a *behavioral simulator*, an *optimizer*, and a space reduction algorithm; the latter one is represented in Fig. 1(a) by the so-called *transistor-level mapping* block.

Starting from the target specifications, and following an approach similar to [13], the *topology generator* creates a database of candidate architectures each of which is addressed by the ordered sequence of resolution bits per stage $b_1 - \cdots - b_k$—see the pipeline diagram of Fig. 1(b). In SNYRCOS all these candidates are sized down to component level (transistors, capacitors,

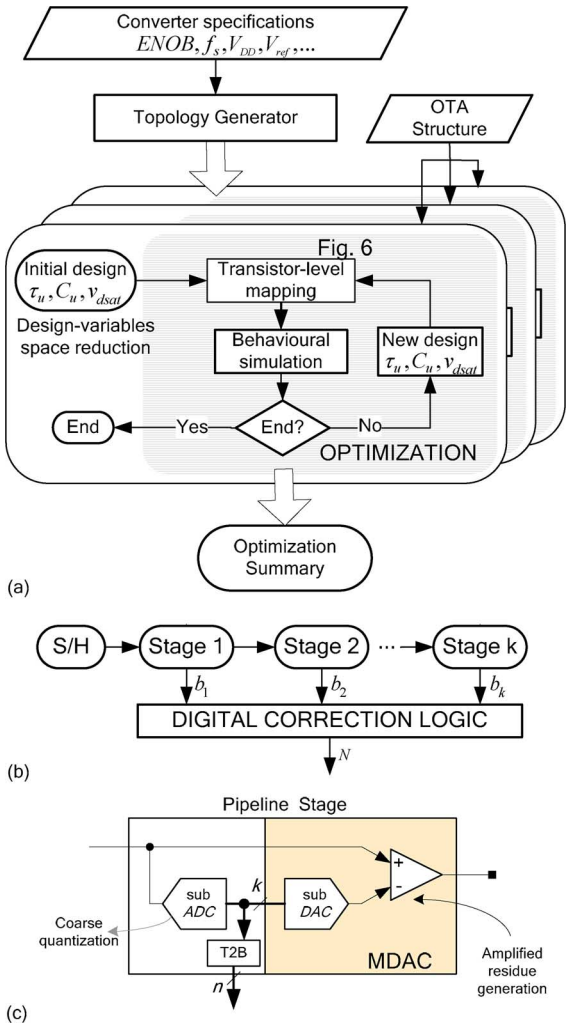


Fig. 1. (a) Basic flow diagram of the synthesis procedure. (b) Pipeline architecture. (c) Detail of a stage.

etc.) by using simulation-based optimization loops [2], [4]. As a difference to previous approaches, this is achieved within very short computation time owing to the concourse of the DSR algorithm. Also, since all candidates architectures are sized down to component level, selection of the best one in terms of power consumption silicon area and robustness is more precise than for previous approaches.

Following each optimization update, SNYRCOS uses a dedicated, *event-driven behavioral simulator*, based on the models presented in [15], to characterize the corresponding converter instance. Similar to other previously reported behavioral models, [5]–[8], those in SNYRCOS employ precalculated, parameterized *closed-form expressions*, instead of *state equations*, to capture the dynamic behavior of the analog blocks. As a difference to previous models, the results provided by our models are very close to those obtained through transistor-level simulations. Actually, our results show less than 0.3-bit deviation in the estimation of the effective converter resolution. This is accomplished by embedding a large number of nonidealities (including small- and large-signal phenomena as well as the impact of parasitics) into the expressions used for behavioral estimations. Obviously, since these expressions change from

one topology to another, event-driven behavioral models are not general-purpose but rather topology- and application-dependent. Currently, SNYRCOS supports single-pole as well as two-stage, two-pole amplifier topologies; other models can be devised following the procedures in [15].

The *space-reduction algorithm* plays two crucial roles in the flow diagram of Fig. 1(a). On the one hand, it reduces the number of independent design variables that must be updated at each iteration of the optimization process. Otherwise, simultaneously handling the dozens of transistor- and component-level parameters involved in a pipeline converter would render any optimization process inefficient and prone to get trapped in local minima. On the other hand, the DSR module employs the values of the independent variable obtained at each step of the optimization process to calculate values for all the parameters involved in the behavioral models.

In order to guarantee technological feasibility of the sized circuits, the DSR module employs information extracted from the technological process to map the three independent variables onto the parameters embedded in the behavioral models. However, instead of using electrical simulations on-the-fly that would compromise the overall computational efficiency of the synthesis flow, such technological information is acquired from *look-up tables* which have been previously generated from batches of Spectre runs. Interestingly enough, this approach inherently captures technology effects (e.g., leakage currents) which are not included in the event-driven behavioral models, thereby combining high speed and accuracy.

The last module in Fig. 1(a), the *optimizer*, is responsible for exploring the reduced design space of each candidate topology and finding the best converter solution. SNYRCOS employs the *adaptive statistical algorithm* procedure reported in [11] which combines *statistical* and *gradient-like* techniques to update parameters along the optimization cycle. The optimization process of a candidate topology starts by guessing an initial design, represented by a set of values of the reduced independent variables. After transistor-level mapping and behavioral simulation, the performance of the converter instance is evaluated according to a spec-dependent *cost function*. Such a cost function can be arbitrarily defined in terms of the overall power consumption of the converter and other common ADC metrics (SNDR, ENOB, SFDR, INL, DNL, ...) [4], [11]. These metrics are readily calculated using a set of postprocessing routines also available in SNYRCOS. After evaluation, a new movement is generated in the reduced design space and the process is repeated again. The outcome of the optimization loop is that particular converter configuration which minimizes the cost function. The same procedure is applied for all candidate topologies and the results are stored in an optimization summary file.

SNYRCOS has been fully integrated into the Matlab-Simulink framework. However, contrary to prior approaches [5]–[8], the behavioral models of the pipeline building blocks have been coded in C language, by means of so-called *S-functions* [19]. This increases computational efficiency. These models have been collected as individual blocks into Simulink libraries so that arbitrary pipeline architectures can be generated by simply interconnecting elements from these libraries.

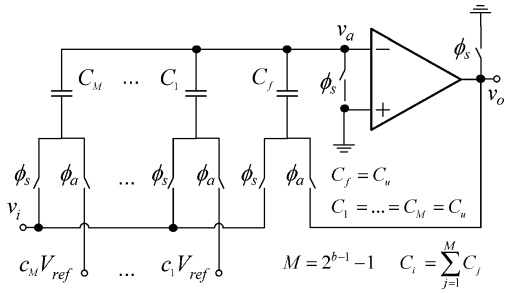


Fig. 2. Schematic-level implementation of the MDAC.

## III. Design Space Reduction Algorithm

The basic purpose of the DSR algorithm is to derive all the pertinent transistor- and component-level parameters of a design from a minimum set of independent variables. In SNYRCOS, this is done by following a *block-based* approach so that a reduced number of running variables are defined for each of the building elements of the ADC [see Fig. 1(b)–(c)], i.e., Sample&Hold (S&H) amplifier, flash sub-ADCs, and Multiplying Digital-to-Analog Converters (MDAC) [13]–[18]. In the following, focus is on the DSR algorithm for the MDAC block [dashed block in Fig. 1(c)], whose basic SC structure is shown in Fig. 2. Note that the algorithm can be similarly applied to S&H amplifiers as they can be simply implemented by removing the $M$ left-most branches of Fig. 2. In order to simplify notation, the position of the MDAC within the pipeline chain is not explicitly indicated in the derivation below—in practice MDACs may be different along the pipeline and SNYRCOS actually accounts for that. Regarding the OTA, we will restrict the analysis to just two alternative OTA topologies, namely: one-stage and two-stage Miller Compensated (MC) OTA topologies. Exemplary OTA realizations for both categories are, respectively, shown in Fig. 3(a) and (b).

Regardless of whether single-stage or two-stage OTAs are employed, the proposed DSR algorithm only requires three independent variables to fully span the component-level parameters of the MDAC, namely:

- the unitary capacitance, $C_u$;
- the time constant, $\tau_u$, of the OTA;
- the saturation voltage of the transistors composing such amplifier, $\{v_{\rm dsat}\}$.

Additionally, the Least Significant Bit (LSB) of each stage, as defined by the topology generator of Fig. 1(a), is employed as a constraint on the maximum error associated to the stage. Regarding the choice of $\{v_{\rm dsat}\}$, it is worth mentioning that transistors are constrained to work in strong inversion and more specifically into saturation region. Hence, the saturation voltage is closely connected to the overdrive voltage $(V_{\rm gs} - V_T)$ and its value provides information about the level of inversion and the transconductance that is achieved for given drain current. In our design we constraint $\{v_{\rm dsat}\}$ to remain larger than 100 mV.

Note that the variables above are typically employed for manual design and, hence, their values are representative for designers to monitor the synthesis process. Basically the unitary capacitance controls errors (typically the larger the capacitance, the smaller the errors) and speed. The time constants together with the capacitances set the transconductances,

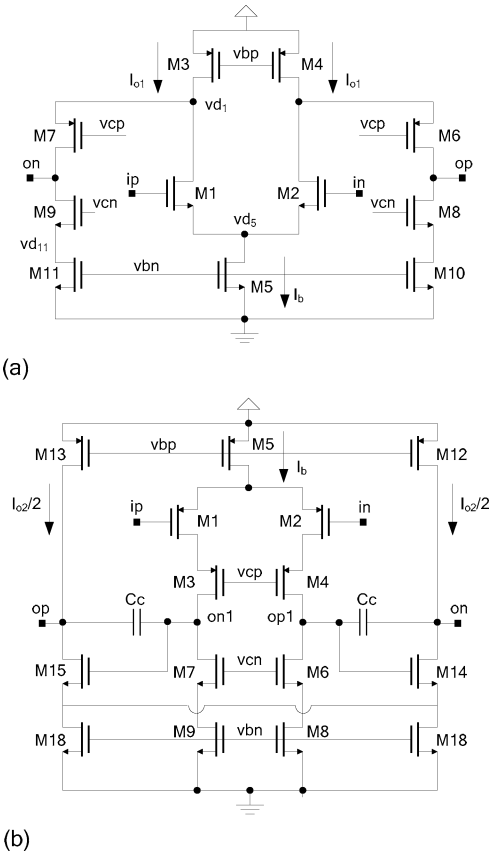


Fig. 3. Examples of OTA topologies considered: (a) one-stage folded cascode and (b) two-stage (first-stage telescopic) MC topologies.

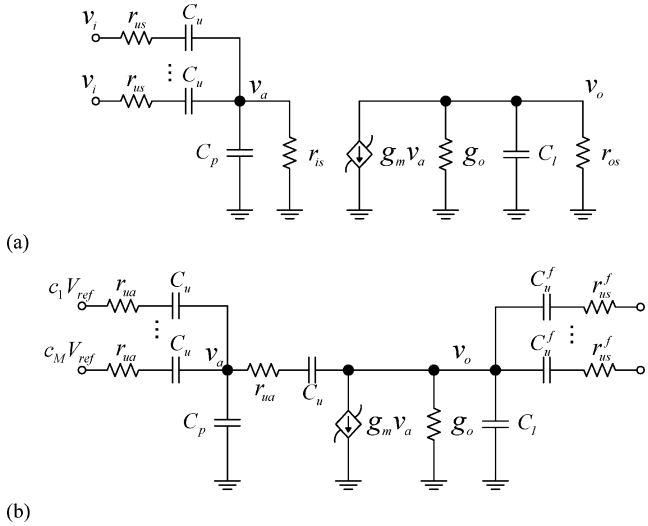


Fig. 4. Equivalent MDAC circuits in: (a) sampling ($\phi_s$ on) and (b) amplification ($\phi_a$ on) phases for a one-stage OTA model. Included small-signal parameters are the transconductance, $g_m$ of the OTA and its output conductance, $g_o$, and the sum of all the grounded capacitances at the input and output terminals of the OTA, denoted as $C_p$ and $C_l$, respectively. Switches in Fig. 1 are replaced by their respective switch-on resistances $r_{\rm us}, r_{\rm ua}, r_{\rm is}, r_{\rm os}$.

and by combining transconductances and transistor saturation voltages one obtains currents. We find convenient using time constants instead of transconductances because they inform about the settling behavior of the OTA and can be equally applied to single- and two-stage topologies [15]. Regarding saturation voltages, it can be guaranteed that all the spanned transistor-level configurations are feasible by defining a suitable range for the saturation voltages of transistors according to the supply conditions of the converter.

From these reduced set of variables the expansion of the design space is made into simple and univocal way.

The design space reduction process is accomplished by, first, imposing a set of constraints derived from small-signal analyses and, second, by running a mapping algorithm to derive the remaining parameters. It is worth noticing that although design space reduction relies on small-signal considerations, the behavioral models employed for performance evaluation and hence for guiding the optimization process, accounts for nonlinear behaviors [17].

### A. Mapping Constraints

They concern the switch-on resistances of the MDAC, as well as, the dc-gain and noise requirements of the OTA.

*1) Switch-On Resistances: Single-Stage OTA Topologies:* Let us first consider single-stage OTA topologies and the corresponding MDAC small-signal models of Fig. 4. The model at the top corresponds to the sampling phase ($\phi_s$ on) while that at the bottom corresponds to the amplification phase ($\phi_a$ on).

Different time constants can be defined for the circuits of Fig. 4(a). During the sampling phase, there are two time constants, one for the input node and the other one for the output node, namely

$$\begin{aligned} \tau_{\rm sa} &= r_{\rm is} \cdot C_{\rm eqs} + r_{\rm us} \cdot C_u \\ \tau_{\rm so} &= r_{\rm os} \cdot C_l \end{aligned} \tag{1}$$

where $C_{\rm eqs} = C_p + C_i + C_f$ stands for the equivalent capacitive load of the amplifier, with $C_i = \sum_{j=1}^{M} C_j$. During the amplification phase [see Fig. 4(b)], each stage of the pipeline is loaded by the next one and, hence, the corresponding time constant depends on parameters of two stages

$$\tau_a = \frac{C_{\rm eqa}}{g_m} + r_{\rm ua} \cdot C_u + r_{\rm us}^f \cdot C_u^f \tag{2}$$

where $r_{\rm us}^f$ and $C_u^f$ model, respectively, the switch-on resistance during the sampling phase and the unitary capacitor of the following stage; $C_{\rm eqa} = C_p + C_i + C_t/\beta$ stands for the equivalent amplifier load; $C_t = C_l + C_i^f$ is the total capacitance load at the output node; and $\beta$ is a feedback factor defined as

$$\beta = \frac{C_f}{C_p + C_i + C_f.} \tag{3}$$

Note that the first term in (2) represents the time constant of the amplifier, i.e.,

$$\tau_u \equiv C_{\rm eqa}/g_m \tag{4}$$

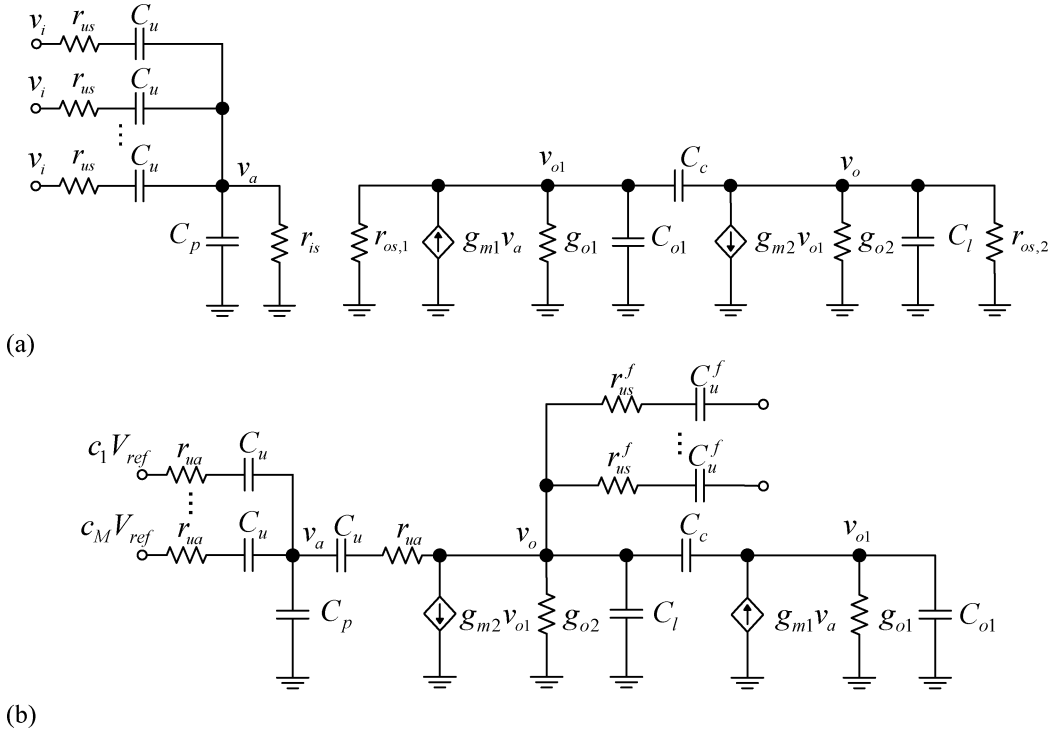


Fig. 5. Equivalent MDAC circuits in: (a) sampling ($\phi_s$ on) and (b) amplification ($\phi_a$ on) phases for a two-stage MC OTA topology. Included small-signal parameters are the transconductances, $g_{m1}$ and $g_{m2}$, and the output conductances, $g_{o1}$ and $g_{o2}$, of the first and second stage of the OTA, respectively, the total grounded capacitance at the output of the first stage, $C_{o1}$, and the compensation capacitance $C_c$. Remaining parameters are defined as in Fig. 4.

which is one of the independent variables selected in the DSR algorithm. Proper operation requires the time constant $\tau_a$ dominates over the rest and, hence, it will be assumed that $\tau_{\rm so} = \tau_{\rm sa} = \alpha \cdot \tau_u$ and $\tau_a = (1+\alpha)\cdot\tau_u$, where $\alpha \ll 1$ (a value of 0.1 is enough for most practical purposes). Accordingly, the switch-on resistances $r_{\rm os}$ and $r_{\rm is}$ can be calculated as

$$\begin{aligned} r_{\rm os} &= \alpha\tau_u/C_l \\ r_{\rm is} &= (\alpha\tau_u - r_{\rm us}\cdot C_u)/C_{\rm eqs}. \end{aligned} \tag{5}$$

Additionally, it will be assumed that

$$r_{\rm us}C_u = r^p_{\rm ua}C^p_u \tag{6}$$

where and $r^p_{\rm ua}$ and $C^p_u$ model, respectively, the switch-on resistance during the amplification phase and the unitary capacitor of the previous stage. Therefore,

$$\begin{aligned} r_{\rm ua} &= \alpha\tau_u/2C_u \\ r_{\rm us} &= r^p_{\rm ua}\cdot C^p_u/C_u. \end{aligned} \tag{7}$$

*2) Switch-On Resistances: Two-Stage OTA Topologies:* In the case of two-stage OTAs (Fig. 5), assuming a critically damped amplifier response [15], the switch-on resistances $r_{\rm os}$ and $r_{\rm is}$ take the form

$$r_{\rm os} = \frac{1+\beta_c\left(1+\frac{C_l}{C_c}\right)}{2\beta_c g_{m2}}$$

$$\times\left(\sqrt{1+\frac{4\alpha\beta_c^2\tau_u g_{m2}/C_c}{\left[1+\beta_c\left(1+\frac{C_l}{C_c}\right)\right]^2}}-1\right)$$

$$r_{\rm is} = (\alpha\tau_u - r_{\rm us}\cdot C_u)/C_{\rm eqs} \tag{8}$$

where $\beta_c = C_c/(C_{o1}+C_c)$. Together with (6), it will be also assumed that

$$r_{\rm os,1} = r_{\rm os,2} \equiv r_{\rm os}. \tag{9}$$

*3) Amplifier DC-Gain:* Assuming a finite dc-gain $A_o$for the amplifier, no matter its particular topology, the output of the MDAC can be expressed as

$$\begin{aligned} v_o &= \frac{1}{1+\varepsilon_g}\left[\frac{C_f+C_i}{C_f}v_i - \sum_{i=1}^{M} c_i V_{\rm ref}\right] \\ &\equiv \frac{1}{1+\varepsilon_g}v_{o,\rm id} \end{aligned} \tag{10}$$

where $\varepsilon_g = 1/(\beta A_o)$ stands for the gain error, and $v_{o,\rm id}$ is the ideal response of the MDAC. From (10), it can be easily inferred that the error voltage due to the finite dc-gain is:

$$\varepsilon_o = v_{o,\rm id} - v_o = \frac{\varepsilon_g}{1+\varepsilon_g}v_{o,\rm id} \approx \varepsilon_g v_{o,\rm id} \tag{11}$$

whose worst-case value is obtained at the reference voltage of the MDAC, i.e.,

$$\varepsilon_{o,\max} = \varepsilon_g \cdot V_{\rm ref} \tag{12}$$

This value must be lower than half LSB of the stage and, therefore, the minimum value for the amplifier dc-gain is given by

$$A_{o,\min} > \frac{2V_{\rm ref}}{\beta \cdot \mathrm{LSB}.} \tag{13}$$

*4) Noise Requirement for the OTA:* The noise contribution of the amplifier, $P_{\rm no}$, must be lower than the quantization noise of the pipeline stage, $P_q$, so that its effective resolution is not limited by noise. On the one hand, the quantization noise is related to the LSB of the stage as [18]

$$P_q = \mathrm{LSB}^2/12. \tag{14}$$

On the other, the noise contribution of the amplifier at the MDAC output can be obtained according to the expression [13]

$$P_{\rm no} = G^2 \cdot S_{\rm op} \cdot \mathrm{BW}_{\rm eq} \tag{15}$$

where $S_{\rm op}$ and $\mathrm{BW}_{\rm eq}$ stand for the noise Power Spectral Density (PSD) and noise equivalent bandwidth of the amplifier [20], respectively; and $G$ models the amplification gain of the MDAC

$$G = (C_f + C_i)/C_f. \tag{16}$$

According to the time constant of the amplifier, the noise equivalent bandwidth can be approximated as [13], [18], [20]

$$\mathrm{BW}_{\rm eq} \approx 1/(4\chi\tau_u) \tag{17}$$

where $\chi = 1$ for single-stage amplifiers and $\chi = 2$ for two-stage MC OTAs, assuming a critically damped response in the equivalent circuit of Fig. 5(b). Replacing (17) into (15), a maximum value for the noise PSD of the amplifier can be extracted

$$P_{\rm no} < P_q \rightarrow S_{\rm op,max} = \frac{\chi\tau_u}{3}\left[\frac{\mathrm{LSB}}{G}\right]^2. \tag{18}$$

Neglecting flicker contributions, the equivalent input noise of an OTA can be modeled as [20][1]

$$S_{\rm op} \approx \frac{8KT}{3g_m}(1+\eta_T) \tag{19}$$

where $\eta_T$ is a topology-dependent noise factor. Hence, by compelling the upper limit on $S_{\rm op}$, a minimum value for the transconductance, $g_m$, can be derived

$$g_{m,\min} = \frac{8 \cdot K \cdot T}{\chi\tau_u}(1+\eta_T)\left[\frac{G}{\mathrm{LSB}}\right]^2. \tag{20}$$

### *B. Mapping Algorithm*

Fig. 6 shows the basic flow diagram of the mapping algorithm. Note that this mapping is realized at each iteration of the optimization routine; i.e., every time the independent variables of the procedure are updated.

[1]In the case of two-stage MC OTA, it is assumed that the noise contribution of the second stage is negligible and, therefore, $g_m$ actually refers to the transconductance of the first stage, $g_{m1}$.

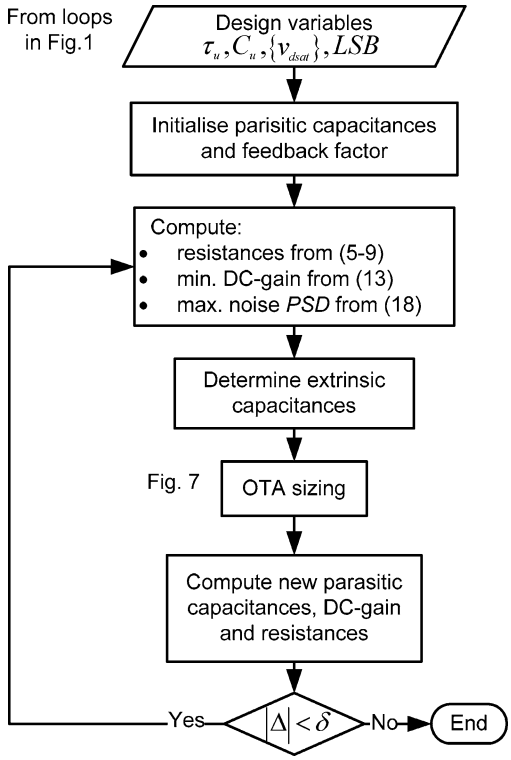


Fig. 6. Synthesis procedure of the MDAC circuit.

The mapping algorithm starts by guessing initial values for the parasitic capacitors $C_p, C_l$, and computing the feedback factor of the amplifier, $\beta$. These capacitances can be expressed as

$$\begin{aligned} C_p &= C_{{\rm pi},i} + C_{{\rm pi},e} \\ C_l &= C_{{\rm po},i} + C_{{\rm po},e} \end{aligned} \tag{21}$$

where $C_{{\rm pi},i}$ and $C_{{\rm po},i}$ (called intrinsic parasitics) agglutinate all the parasitics that load the input and output nodes of the OTA, respectively; whereas, $C_{{\rm pi},e}$ and $C_{{\rm po},e}$ are the extrinsic OTA capacitances at these nodes. Using these values, the switch-on resistances, minimum dc-gain, $A_{o,\min}$, and maximum noise PSD of the OTA, $S_{\rm op,max}$, are calculated from the equations derived in the previous subsection. Once the resistances values are known, the extrinsic parasitic components, $C_{{\rm pi},e}$ and $C_{{\rm po},e}$, are computed and, afterwards, the OTA is fully sized at the electrical level. This allows to precisely derive the parasitic capacitances as well as to update the values of the switch-on resistances, required finite dc-gain and noise PSD. If discrepancies between these values and those originally estimated are higher than a user-defined tolerance value, $\delta$, the procedure is repeated again until convergence is achieved. It is worth observing that this loop precludes deviations between the behavioral and electrical-level description of the MDAC.

The OTA sizing routine, assuming a single-stage topology, is depicted in Fig. 7—a similar routine has been also devised for two-stage MC OTAs [15]. The parameters required by the routine are the unitary capacitor, $C_u$; the time-constant of the OTA, $\tau_u$; the saturation voltages of the transistors $\{v_{\rm dsat}\}$; the extrinsic parasitic capacitances, $C_{{\rm pi},e}, C_{{\rm po},e}$; the minimum

TABLE I
LOOK-UP TABLES USED IN THE DSR ALGORITHM

| Return value | Look-up Table | Comment |
|---|---|---|
| $W$ | $W_g(g_m; L, v_{dsat})$ | Estimate transistor width given the transconductance, length and saturation voltage. By simple matrix manipulation it can be also used to extract the transistor transconductance from remaing parameters, i.e., $g_m = g_m(W; L, v_{dsat})$. |
| $I_{ds}$ | $I_{ds}(W; L, v_{dsat})$ | Estimate the transistor drain-source current given the width, length and saturation voltage. By simple matrix manipulation it can be also used to extract the transistor width from remaing parameters, i.e., $W = W_i(I_{ds}; L, v_{dsat})$. |
| $[C_{gg}, C_{dd}, C_{ss}]$ | $C_{par}(W, L)$ | Estimate MOS terminal parasitic capacitances from the transitor sizes |
| $g_{ds}$ | $g_{ds}(I_{ds}, L, v_{dsat}, V_{ds})$ | Estimate the MOS output conductance given the drain-source current, length, saturation voltage and drain-source voltage |
| $g_{mb}$ | $g_{mb}(g_m, V_{bs})$ | Estimate the NMOS bulk transconductance given the transconductance and source-bulk voltage |

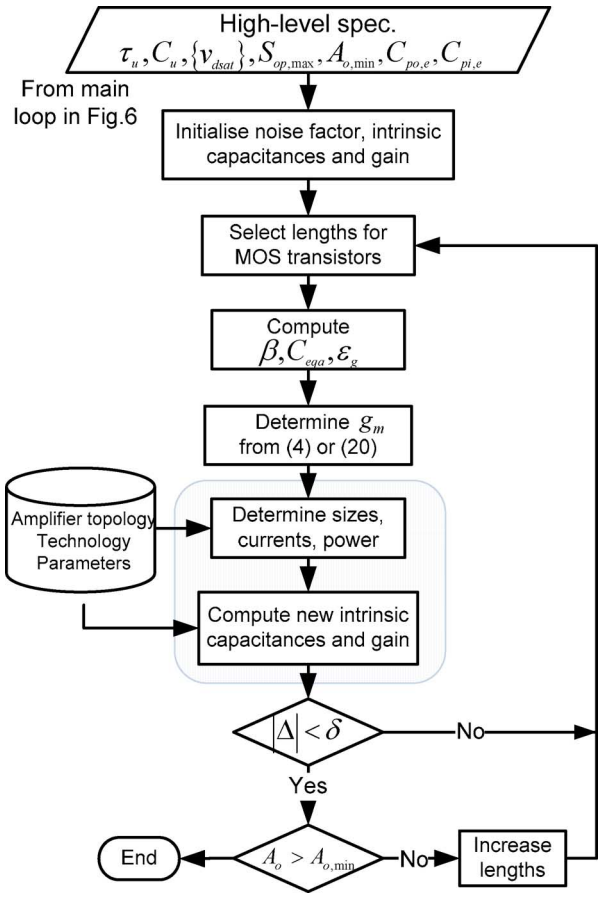


Fig. 7. OTA sizing routine for single-stage OTAs.

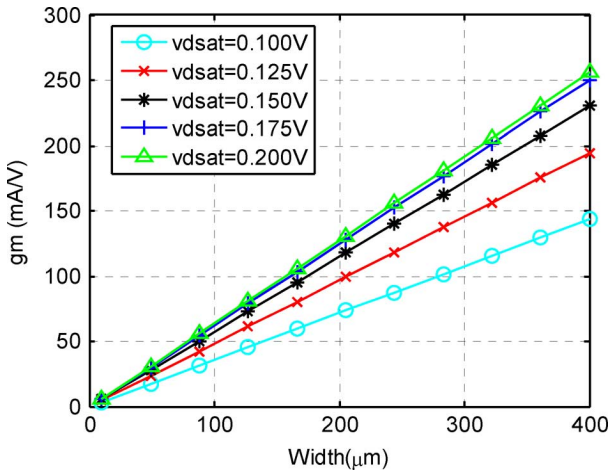


Fig. 8. Simulated transconductance for a 130 nm NMOS transistor in the target technology.

dc-gain, $A_{o,\min}$; and the maximum noise PSD, $S_{\mathrm{op,max}}$. All this information is inherited from the loop of Fig. 6.

The procedure follows an iterative approach which starts by guessing initial values for the intrinsic components $C_{\mathrm{pi},i}$ and $C_{\mathrm{po},i}$; finite dc-gain, $A_o$; topology-dependent noise factor, $\eta_T$; and transistor lengths. Using these values, the feedback factor, $\beta$; gain error factor, $\varepsilon_g$; and equivalent load, $C_{\mathrm{eqa}}$, are evaluated. Then, the minimum value for the transconductance $g_m$ is computed by taking into account speed (4) and noise (20) requirements, whatever more restrictive. With these data, together with the previously planned saturation voltages $\{v_{\mathrm{dsat}}\}$, the sizes and biasing conditions of the OTA MOS transistors are calculated by using the procedure described in the next subsection.

At this point, the overall power consumption of the OTA can be estimated. In the next step, the intrinsic parasitic capacitances are newly calculated and compared to those previously assumed. If discrepancies are higher than a user-defined tolerance value, $\delta$, the iterative process is repeated again until convergence is reached. Finally, if the estimated dc-gain, $A_o$, is lower than the required one, $A_{o,\min}$, the lengths of MOS transistors are increased and the algorithm is repeated again.

It is worth mentioning that despite the iterative nature of the design procedure, it only takes three or four iterations to converge. Also, it is interesting to observe that no *ad hoc* fitting parameter needs to be adjusted in the design procedure.

### C. Calculation of MOS-Related Parameters

In the proposed DSR algorithm, MOS-related parameters are extracted from look-up tables obtained from batches of Spectre simulations in the selected technology. In such simulations, both the dimensions and operating conditions of NMOS and PMOS transistors are varied and the characteristics which are pertinent for the sizing procedure of Fig. 7 (e.g., transconductance or parasitic capacitances) are stored in multidimensional arrays. Such information is later accessed during circuit sizing (potentially

TABLE II
TRANSISTOR-LEVEL OTA SIZING PROCEDURE FOR THE TOPOLOGY IN FIG. 3(A)

| Step | Design equation / Constraint | Comment |
|---|---|---|
| 1 | $W_1 = W_g(g_{m1}; L_1, v_{dsat1})$ | Compute the width and drain current of the transistors in the differential pair from input specifications. |
| 2 | $I_1 = I_{ds}(W_1; L_1, v_{dsat1})$ | |
| 3 | $I_b = 2 \cdot I_1 \quad I_{o1} = 1.2 \cdot I_b$ | Avoid zero current in cascodes. |
| 4 | $W_3 = W_i(I_{o1}; L_3, v_{dsat3}) \quad W_5 = W_i(I_b; L_5, v_{dsat5})$<br>$W_7 = W_i(I_{o1} - I_1; L_7, v_{dsat7}) \quad W_9 = W_i(I_{o1} - I_1; L_9, v_{dsat9})$<br>$W_{11} = W_i(I_{o1} - I_1; L_{11}, v_{dsat11})$ | Derive remaining transistor widths. |
| 5 | $[C_{gg1}, C_{dd1}, C_{ss1}] = C_{par}(W_1, L_1) \quad [C_{gg7}, C_{dd7}, C_{ss7}] = C_{par}(W_7, L_7)$<br>$[C_{gg9}, C_{dd9}, C_{ss9}] = C_{par}(W_9, L_9) \quad C_{pi,i} = C_{gg1} \quad C_{po,i} = C_{dd7} + C_{dd9}$ | Compute intrinsic parasitic capacitances. |
| 6 | $V_{d1} = V_{dd} - v_{dsat3} - 50\text{mV} \quad V_{d5} \approx V_{cmi} - v_{dsat1} \quad V_{d11} = v_{dsat11} + 50\text{mV}$ | $M_3$ and $M_{11}$ biased 50mV over the saturation voltage to maximize the output swing. |
| 7 | $V_{ds1} = V_{d1} - V_{d5} \quad V_{sd3} = V_{dd} - V_{d1} \quad V_{sd7} = V_{d1} - V_{cmo}$<br>$V_{ds9} = V_{cmo} - V_{d11} \quad V_{ds11} = V_{d11}$ | Calculate the drain-source voltages. |
| 8 | $g_{ds1} = g_{ds}(I_1, L_1, v_{dsat1}, V_{ds1}) \quad g_{sd3} = g_{ds}(I_{o1}, L_3, v_{dsat3}, V_{sd3})$<br>$g_{sd7} = g_{ds}(I_{o1} - I_1, L_7, v_{dsat7}, V_{sd7}) \quad g_{ds9} = g_{ds}(I_{o1} - I_1, L_9, v_{dsat9}, V_{ds9})$<br>$g_{ds11} = g_{ds}(I_{o1} - I_1, L_{11}, v_{dsat11}, V_{ds11})$<br>$g_{m3} = g_m(W_3; L_3, v_{dsat3}) \quad g_{m7} = g_m(W_7; L_7, v_{dsat7})$<br>$g_{m9} = g_m(W_9; L_9, v_{dsat9}) \quad g_{m11} = g_m(W_{11}; L_{11}, v_{dsat11})$ | Compute the transconductances and output conductances of transistors. |
| 9 | $A_o \approx \frac{g_{m1} g_{m7} g_{m9}}{g_{ds11} g_{ds9} g_{m7} + (g_{ds1} + g_{sd3}) g_{sd7} g_{m9}} \quad P = 2 \cdot I_{o1} \cdot V_{dd} \quad \eta_T = \frac{g_{m3} + g_{m9}}{g_{m1}}$ | Calculate the DC-gain, power consumption and topology-dependent noise factor of the OTA |

TABLE III
SYNTHESIS RESULTS FOR DIFFERENT PIPELINE ARCHITECTURES

| Stages | Resolution-per-stage | Power consumption (mW) |
|---|---|---|
| 5 | 2-3-3-3-3 | 18.49 |
| 5 | 3-2-3-3-3 | 17.21 |
| 5 | **3-3-3-3-2** | 16.13 |
| 6 | 2-2-2-3-3-3 | 21.73 |
| 6 | 3-2-3-2-2-3 | 17.65 |
| 6 | 3-3-3-2-2-2 | 17.57 |
| 7 | 2-2-2-3-3-3-2 | 24.65 |
| 7 | 3-2-3-2-2-2-2 | 18.89 |
| 7 | 3-2-2-2-2-2-3 | 24.53 |
| 7 | 3-3-2-2-2-2-2 | 18.91 |
| 8 | 2-2-2-2-2-2-2-3 | 27.98 |
| 8 | 3-2-2-2-2-2-2-2 | 20.06 |
| 9 | 2-2-2-2-2-2-2-2-2 | 25.60 |

TABLE IV
CORNERS DEFINITIONS

| | Typical | Fast | Slow | Worst ONE | Worst ZERO |
|---|---|---|---|---|---|
| MOS models | Typ | Fast *n*<br>Fast *p* | Slow *n*<br>Slow *p* | Fast *n*<br>Slow *p* | Slow *n*<br>Fast *p* |
| Temperature | 27ºC | -40ºC | 85ºC | 85ºC | 85ºC |
| Cap. models | Typ | Min | Max | Typ | Typ |
| Volt. supply | 1.2V | 1.32V | 1.08V | 1.08V | 1.08V |

requiring some interpolation techniques) based upon the values of the variables which are handled by the mapping algorithm. Thus, for instance, given the length and saturation voltage of a transistor, the channel width required for a specific transconductance can be readily calculated by means of a look-up table of the type $W = W_g(g_m; v_{\rm dsat}, L)$. Other tables used in the DSR algorithm, generated for both NMOS and PMOS transistors, are listed in Table I.

Note that look-up tables are filled with data obtained from simulations of complex BSIM models and, hence, they intrinsically capture small-dimensions phenomena. Otherwise stated, although the DSR algorithm handles a reduced set of variables, this does not overlook any of the deep-submicrometer effects observed in modern technological processes. Therefore, the approach is virtually suitable for any technology. Anyhow, it is always convenient to apply simplifications which help to speed-up the DSR algorithm. For instance, in the used 130 nm CMOS technology, it has been found that parameters $W$ and $g_m$ follow an almost linear relationship (deviations smaller than 0.05%) for given values of $L$ and $v_{\rm dsat}$. This is illustrated in Fig. 8, which plots $g_m$ versus $W$ for different $v_{\rm dsat}$ values, assuming a minimum length NMOS transistor. In such a case, it has been assumed with negligible error that $W = W_g(g_m; v_{\rm dsat}, L) \approx K(v_{\rm dsat}, L) \cdot g_m$ thus, decreasing the dimensionality of the look-up table. As an illustration, (22) at the bottom of the next page shows an excerpt of the $K(v_{\rm dsat}, L)$ table (in units of mV·m/A) in the referred technology.

Once the technology has been characterized, the transistor-level sizing of the selected OTA topology (shaded area in Fig. 7) can be carried out. For illustration purposes, Table II shows the

TABLE V
SIZING RESULTS FOR THE 5-STAGE 3-3-3-3-2 PIPELINE ADC

| Parameters | | S&H | MDAC1 | MDAC2 | MDAC3 | MDAC4 |
|---|---|---|---|---|---|---|
| Seed variables | Unitary capacitance $C_u$(pF) | 4 | 0.35 | 0.2 | 0.1 | 0.1 |
| | Time Constant $\tau_u$ (nS) | 0.435 | 0.625 | 0.75 | 1.10 | 1.4 |
| | Saturation voltage $v_{dsat}$(V) | 0.10 | 0.10 | 0.10 | 0.10 | 0.10 |
| Sizes and biasing conditions | $W_{1,2}/L_{1,2}$ (µm/µm) | 95/0.3 | 177.6/0.3 | 120/0.3 | 60/0.3 | 40/0.3 |
| | $W_{3,4}/L_{3,4}$ (µm/µm) | 95/0.3 | 177.6/0.3 | 120/0.3 | 60/0.3 | 40/0.3 |
| | $W_5/L_5$ (µm/µm) | 128/0.2 | 208/0.2 | 144/0.2 | 64/0.2 | 48/0.2 |
| | $W_{6,7}/L_{6,7}$ (µm/µm) | 12/0.2 | 18/0.2 | 13/0.2 | 6/0.2 | 5/0.2 |
| | $W_{8,9}/L_{8,9}$ (µm/µm) | 12/0.2 | 18/0.2 | 13/0.2 | 6/0.2 | 5/0.2 |
| | $W_{12,13}/L_{12,13}$ (µm/µm) | 688/02 | 352/0.2 | 256/0.2 | 176/0.2 | 64/0.2 |
| | $W_{14,15}/L_{14,15}$ (µm/µm) | 135/0.2 | 75/0.2 | 50/0.2 | 36/0.2 | 16/0.2 |
| | $W_{18}/L_{18}$ (µm/µm) | 360/02 | 146/0.2 | 140/0.2 | 92/0.2 | 36/0.2 |
| | $r_{us}\|r_{is}\|r_{ua}\|r_{oa}(\Omega)$ | 50 \| 50 \| 50 \| 50 | 600 \| 200 \| 600 \| 150 | 1000 \| 200 \| 1000 \| 250 | 1000 \| 750 \| 1000 \| 450 | 1000 \| 1000 \| 1000 \| 800 |
| | Comp. cap. ($C_c$) (pF) | 1.9 | 0.9 | 0.65 | 0.4 | 0.4 |
| | $I_b\|I_{o2}$ (mA) | 0.309 \| 4.087 | 0.503 \| 2.105 | 0.35 \| 1.55 | 0.16 \| 1.05 | 0.11 \| 0.45 |
| Derived parameters (typical operation conditions) | $A_o\|A_{o1}\|A_{o2}$ | 4375 \| 287 \| 15 | 4852 \| 315 \| 15 | 4648 \| 308 \| 15 | 5144 \| 342 \| 15 | 4919 \| 308 \| 16 |
| | $g_{m1}\|g_{m2}$ (mA/V) | 2.466 \| 27.35 | 4.212 \| 14.4 | 2.901 \| 10.27 | 1.343 \| 7.067 | 0.992 \| 3.06 |
| | Eq. input noise(nV/√Hz) | 4.41 | 3.27 | 3.98 | 5.74 | 6.91 |
| | GBW (MHz) | 180 | 620 | 589 | 438 | 340 |
| | Phase Margin (degrees) | 59.1 | 3.9 | 4.71 | 6.5 | 7.94 |
| | $C_{pi}\|C_{po1}\|C_{po2}$ (fF) | 212 \| 747 \| 951 | 387 \| 625 \| 733 | 263 \| 552 \| 631 | 131 \| 446 \| 591 | 88 \| 399 \| 484 |
| | $C_{eqa}$(pF) | 6.247 | 25.71 | 23.25 | 26.15 | 13.2 |
| | $\beta\|\beta_c$ | 0.909 \|0.718 | 0.180 \| 0.590 | 0.164 \| 0.541 | 0.151 \| 0.473 | 0.162 \| 0.501 |
| | Power cons.(mW) | 5.506 | 3.381 | 2.522 | 1.731 | 0.890 |

TABLE VI
ELECTRICAL SIMULATIONS OF THE SYNTHESIZED CONVERTER

| Stage | ENOB | | | | |
|---|---|---|---|---|---|
| | Typical | Fast | Slow | Worst ONE | Worst ZERO |
| Pipeline | 9.73 | 9.74 | 9.00 | 9.58 | 9.48 |
| S&H | 10.6 | 11.1 | 10.8 | 10.4 | 9.92 |
| Stage 1 | 9.22 | 9.25 | 9.13 | 9.05 | 9.04 |
| Stage 2 | 8.79 | 8.83 | 8.74 | 8.71 | 8.53 |
| Stage 3 | 8.15 | 8.22 | 7.64 | 7.95 | 7.79 |
| Stage 4 | 8.23 | 8.33 | 8.21 | 7.85 | 7.35 |

procedure for sizing the OTA of Fig. 3(a). For simplicity, it has been assumed that the bulk transconductance of all the transistors is null. As can be seen, using the parameters inherited from Fig. 7, the procedure obtains the dimensions and biasing conditions of the transistors, the intrinsic parasitic capacitances of the OTA, as well as its dc-gain, power consumption and input-referred noise.

## IV. SYNTHESIS OF A 10 BITS@60 MS/S PIPELINE ADC

The synthesis tool described in Section II has been used to design a 10-bit@60 MS/s@1.2 V pipeline ADC in a 0.13 $\mu$m CMOS technology. Due to the reduced voltage supply, a two-stage MC amplifier topology, shown in Fig. 3(b), has been chosen for the realization of the S&H and MDACs. For similar reasons, the architecture exploration of Fig. 1(a) has been restricted to pipelines with a maximum of 3 bits per stage.

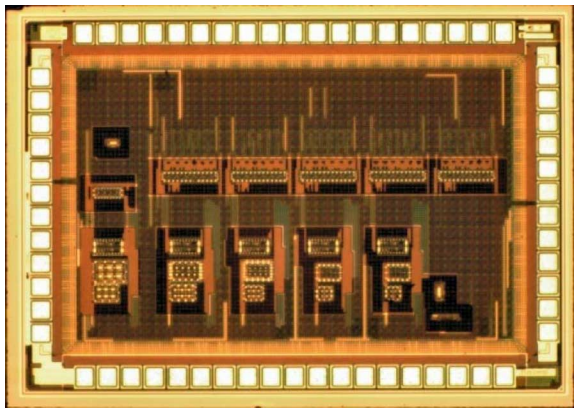

Fig. 9. Chip microphotograph of prototype ADC.

Thirteen different pipeline architectures have been synthesized down to transistor-level, assuming typical operation conditions. In all cases, the cost function has been formulated so as to reduce the power consumption of the candidate architecture, constrained to obtain at least 9-bits of effective resolution at Nyquist rate. Results are listed in Table III. The exploration and synthesis process takes about 25 minutes of CPU time (using a 2.5 GHZ@3 GB RAM INTEL processor) and 650 iterations per topology.

Table III reveals that the 5-stage pipeline architecture with 3-3-3-3-2 bits-per-stage distribution achieves the lowest power consumption, slightly above 16 mW. Considering this topology

$$K = \begin{array}{c} v_{\mathrm{dsat}}(V) \rightarrow \\ \\ \\ \\ \end{array} \begin{array}{c} \begin{array}{ccccc} 0.100 & 0.125 & 0.150 & 0.175 & 0.200 \end{array} \\ \begin{bmatrix} 2.78 & 2.05 & 1.73 & 1.59 & 1.56 \\ 4.99 & 3.59 & 2.91 & 2.54 & 2.32 \\ 8.39 & 5.95 & 4.77 & 4.08 & 3.64 \\ 11.72 & 8.43 & 6.70 & 5.66 & 5.02 \end{bmatrix} \end{array} \begin{array}{c} L(\mathrm{nm}) \\ 130 \\ 200 \\ 300 \\ 400 \end{array}. \tag{22}$$

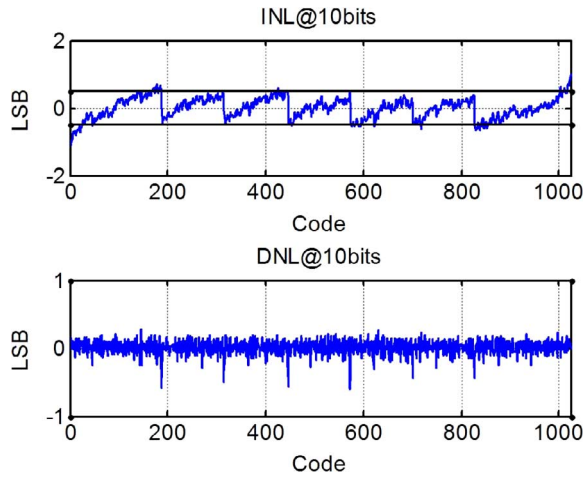


Fig. 10. INL and DNL of the pipeline ADC.

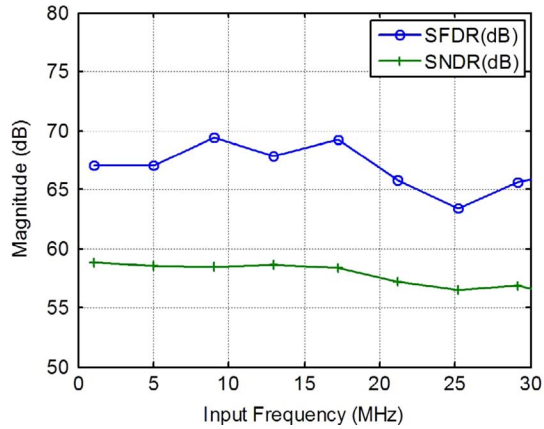


Fig. 11. SFDR and SNDR versus input frequency measured at 27° and 1.2 V supply.

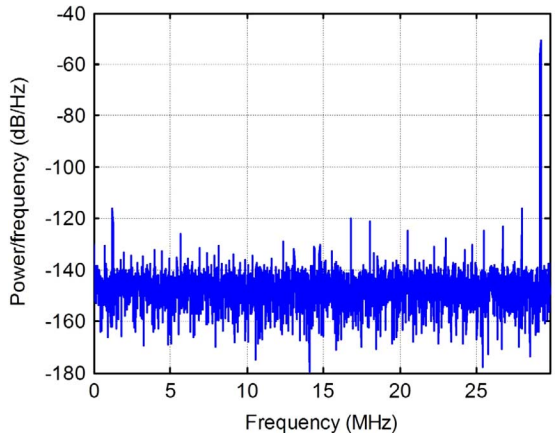


Fig. 12. ADC power spectrum with 28 MHz tone.

TABLE VII
PERFORMANCE SUMMARY OF THE CONVERTER

| | |
|---|---|
| Technology | 0.13µm, 6Metal |
| Resolution | 10 bits |
| Conversion Rate | 60MS/s |
| Supply Voltage | 1.2V (1.08 – 1.32V) |
| Temperature | 25º (-40 – 85º) |
| Input range | $0.8V_{pp}$ |
| DNL | -0.60/0.28 LSB |
| INL | -0.61/0.61 LSB |
| ENOB | 9.47bits @ 1MHz<br>9.15bits @ 28MHz |
| SNDR | 58.77dB @ 1MHz<br>56.84dB @ 28MHz |
| SFDR | 67.05dB @ 1MHz<br>65.64dB @ 28MHz |
| Area (including pads) | $3mm^2$ |
| Total power (Analog/digital +I/O) | 23mW |
| FOM | 0.54pJ/conv @ 1MHz<br>0.67pJ/conv @ 28MHz |

for final design, the converter was simulated with Spectre under different Process, Voltage, and Temperature (PVT) corners. Such corners are defined in Table IV. The specifications were satisfied on three corners (including the typical), but failed in the other two. In order to guarantee the robustness of the design under all operating conditions, SNYRCOS was used again to redesign the converter. To this end, the time constants of the pipeline stages were slightly decreased while keeping the unitary capacitors and the saturation voltages unaltered. Owing to the computational efficiency of the proposed synthesis tool this only takes a few seconds, as it requires running the algorithm of Fig. 6 just once. Along the synthesis process, extrinsic parasitic capacitances were realistically estimated based on layouts of structures such as switches, MiM capacitors or metal strips, as well as on the preliminary sizings obtained during topology exploration. Discrepancies with final routing parasitics were evaluated and taken into account in a new redesign cycle with SNYRCOS, which required some minor modifications on the transistor dimensions. After the PVT and layout redesigns, the converter exhibits a power consumption increment of 3 mW.

Table V summarizes the final sizing results, including transistor dimensions and biasing conditions, of the MDACs and the S&H amplifier of the architecture 3-3-3-3-2. The parameters in the dashed rows of Table V are the independent variables of the DSR algorithm described in Section III. OTAs have been sized so as to obtain a stable critically damped MDAC closed-loop response. Accordingly, the smaller the feedback factor of the OTAs, the lower the required phase margins [15]. The pipeline core has been validated with electrical-level simulations. Table VI shows the Effective Number Of Bits (ENOB) obtained with SPECTRE simulations for the pipeline converter and its stages, at the different corners defined in Table IV. These results are in close agreement with SNYRCOS simulations (deviations lower than 0.3-bit in effective resolution were obtained) and confirm the robustness of the design.

The chip microphotograph of prototype ADC is shown in Fig. 9. Besides the pipeline core, the layout includes generators for the voltage references used to define the full-scale converter range and the common-mode voltage of the OTAs. Also, the prototype integrates digital circuitry, a clock generation and distribution network, and an internal reference current generator to bias the OTAs and the sub-ADCs. These blocks increase the power consumption of the converter by about 4 mW. The chip occupies about 3 $mm^2$, including pads.

The experimental Integral Nonlinearity (INL) and Differential Nonlinearity (DNL) results are plotted in Fig. 10. They

TABLE VIII
PERFORMANCE COMPARISON WITH PUBLISHED WORKS

| Ref | Bits | $ENOB@f_i$ (bits @ MHz) | $f_s$ (MS/s) | Process | Supply (V) | Area ($mm^2$) | Power (mW) | FOM (pJ/conv) | Technique[1] |
|---|---|---|---|---|---|---|---|---|---|
| [21] | 10 | 9.03@24.5 | 50 | 0.18µm | 1.8 | 0.86 | 12.0 | 0.46 | RSH, OPSH, OTH |
| [22] | 10 | 8.51@12.5 | 25 | 0.13µm | 1.2 | 0.8 | 4.8 | 0.53 | OTH |
| [23] | 14 | 11.60@1 | 20 | 0.18µm | 2.8 | 1.15 | 34.8 | 0.56 | CAL |
| [24] | 10 | 9.03@10 | 100 | 0.18µm | 1.8 | 1.28 | 31.0 | 0.59 | OPSH |
| **This work** | **10** | **9.15@28** | **60** | **0.13µm** | **1.2** | **3** | **23** | **0.67** | **CLA** |
| [25] | 8 | 7.68@99 | 200 | 0.18µm | 1.8 | 0.15 | 30.0 | 0.73 | SWO |
| [26] | 10 | 8.66@79 | 205 | 90nm | 1.0 | 1 | 61.0 | 0.74 | OTH |
| [27] | 10 | 8.80@20 | 50 | 0.18µm | 1.8 | 1.43 | 18.0 | 0.81 | OPSH |
| [28] | 10 | 8.53@50 | 100 | 90nm | 1.0 | 4.03 | 30.0 | 0.81 | OTH |
| [29] | 14 | 11.34@50 | 100 | 90nm | 1.2 | 1 | 250.0 | 0.97 | CAL |
| [30] | 10 | 8.84@30 | 60 | 0.35µm | 1.5 | 5.76 | 28.9 | 1.05 | OTH |
| [31] | 10 | 9.24@10.7 | 30 | 0.18µm | 1.8 | 0.7 | 21.6 | 1.19 | RSH,OPSH |
| [32] | 14 | 10.41@1 | 40 | 0.18µm | 2.8 | 1.15 | 72.8 | 1.34 | CAL |
| [33] | 10 | 8.51@25 | 50 | 0.18µm | 1.8 | 1.1 | 27.0 | 1.48 | RSH |
| [34] | 10 | 9.26@100 | 170 | 0.18µm | 3.3 | 0.85 | 180.0 | 1.73 | OPSH |
| [35] | 8 | 7.03@4.9 | 10 | 90nm | 0.5 | 0.855 | 2.4 | 1.83 | RSH |
| [36] | 10 | 9.01@10 | 20,48 | 0.35µm | 1.5 | 1.3 | 19.5 | 1.85 | CLA |
| [37] | 12 | 10.26@37.5 | 75 | 0.35µm | 3.0 | 7.9 | 284.0 | 3.10 | CAL |
| [38] | 13 | 10.84@1 | 43 | 0.18µm | 1.8 | 3.6 | 268.0 | 3.41 | CAL |
| [39] | 10 | 8.84@15 | 30,4 | 0.35µm | 3.3 | 1.47 | 52.0 | 3.72 | CLA |
| [40] | 13 | 10.00@76 | 180 | 0.25µm | 3.3 | 15 | 756.0 | 4.10 | RSH |
| [41] | 15 | 11.50@10 | 20 | 0.18µm | 1.8 | 3.91 | 280.0 | 4.83 | CAL |
| [42] | 8 | 5.85@20 | 100 | 0.18µm | 1.0 | 2.04 | 30.0 | 5.19 | SWO |
| [43] | 5 | 3.96@300 | 600 | 0.18µm | 1.8 | 0.27 | 70.0 | 7.50 | CAL |

[1] RSH: Removing SH · OPSH: Opamp sharing · OTH: Other technique · CAL: Calibration · CLA: Classical · SWO: Switched-opamp

both remain well below 1 LSB and, hence, the converter monotonicity is guaranteed. Fig. 11 represents the SFDR and SNDR of the converter versus input signal frequency at typical operation conditions. As can be observed, the effective resolution of the converter remains above 9 bits (SNDR above 56 dB) along the whole Nyquist band. As an illustration, Fig. 12 shows the ADC output spectrum for a full-scale 28 MHz tone. The same smooth behavior of the converter were also observed under two different operation conditions, namely, a fast case with $-40°$ and 1.32 V supply; and a slow case with 85° and 1.08 V supply.

Table VII summarizes the ADC performance, where, $\mathrm{FOM} = P/(2^{\mathrm{ENOB}} \cdot f_s)$, $P$ is the power consumption, and $f_s$ is the sampling frequency. Finally, Table VIII compares the FOM of this design with other recent silicon-proven converters published in most prestigious forums. As can be seen, our design obtains a FOM comparable to other realizations which employ specific power reduction strategies such as, opamp sharing, S&H-less design or switched-opamp techniques. This demonstrates the efficiency and reliability of our proposed design methodology.

## V. CONCLUSION

A synthesis tool for the design of pipeline ADCs has been presented. It is based on the combination of an accurate behavioral simulator, a simulated-annealing optimizer and a design-space reduction algorithm. The proposed tool is able to synthesize pipeline ADCs in very short design times, in the order of minutes, while obtaining an excellent agreement between behavioral- and electrical-level simulations. The procedure has been demonstrated with the design of a 10 bits@60 MS/s@1.2 V pipeline ADC in a 0.13 $\mu$m CMOS technology. This converter obtains a FOM in the state-of-the-art, in spite that no specific power reduction strategy has been employed.

The advantages of this approach can be summarized in the following points.

- Design space exploration relies on comparison of fully sized instances and hence topology selection is quite certain.
- Parasitic effects are intrinsically considered in the design flow thus reducing the need of bottom-up refinements.
- High- and low-level specifications mapping are combined in a single step, thus drastically reducing the design cycle and the number of user iterations.
- The necessity to overestimate building block requirements is reduced.
- It strongly relies on circuit design considerations rather than sophisticated mathematical algorithms. This gives the user a closer insight on the design task.

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